COMPUTER AND CONTROL ENGINEERING

Manufacturing and In-Field Testing Techniques

Funded By	Dipartimento DAUIN FONDAZIONE CRT CASSA DI RISPARMIO DI TORINO [P.iva/CF:06655250014]

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Context of the research activity	Nowadays, the number of integrated circuits included in critical environments such as the automotive field is continuously growing. For this reason, semiconductor manufacturer has to guarantee the reliability of the released components for the entire life-cycle that can be up to 10 -15 years. Quality is achieved by a combination of good manufacturing test practices and in-field detection techniques. The activities planned for this proposal includes efforts towards the Manufacturing and In-Field Testing Techniques for Automotive oriented Systems-on-Chip (SoC): - Study and development of innovative Fault Simulation strategies that could manage current SoC designs complexity - Implementation of Silicon Diagnosis techniques based on ad-hoc test equipment development. - The design of test strategies aimed at supporting in-field error detection and malfunctioning information collection, which are demanded by recent standards such as the ISO-26262 and researched by the leading companies of the Automotive Market. The project will enable a phd student to work on a very timely subject and supported by companies currently collaborating with the research group. Expectation is to actively contribute to next generation chip reliable design. The potential outcome of the project is both related to industrial advances and high quality publication.

	Research objectives The phd student will pursue objectives in the broader research field of the Automotive Reliability and Testing. Key enabling factor for this work is the availability of a setup that includes both netlists to be simulated and real silicon chips with development boards to effectively use.

Objectives	Innovative Fault Simulation strategies In this research field, the phd student will look into the following directions: • Setup of a low-cost test scenario based on low-cost equipment and computational infrastructure. 1. Design and implementation of a tester able to effectively drive the test and diagnosis procedure 2. Logic diagnosis based on the collected results on a set of failing devices 3. Provide information to Failure Analysis labs for a faster identification of the root cause of a malfunctioning • Conception of techniques that exploits the real silicon to accelerate simulation and fault simulation processes. 1. Enabling fast prototyping of functional procedures to be graded via logic simulation 2. Injecting faults through the design for testability features Silicon Diagnosis techniques This research subject is supported by the availability of some failing devices identified as faulty during the manufacturing tests. Activities will be the following: • Reproduction of the faulty behavior by exploiting several methods 1. Direct stimulation of the scan chain and other Design for Testability mechanisms like Built-In Self-Test 2. Accurately generated Functional programs execution • Usage and development of EDA tools to 1. Perform a logic investigation about the location and nature of faults affecting the population of faulty chips 2. Refine test patterns to achieve a faster detection In-field error detection and malfunctioning information collection Development of methods for achieving high coverage of defects appearing along with mission behavior as demanded by the ISO-26262 1. Key-on and runtime execution of Software-based Self-Test procedure 2. Diagnosis trace for faster failure analysis of returns from fields.

Skills and competencies for the development of the activity	Firmware, software, EDA tools, Simulation, Netlist design, Automatic Test Equipment